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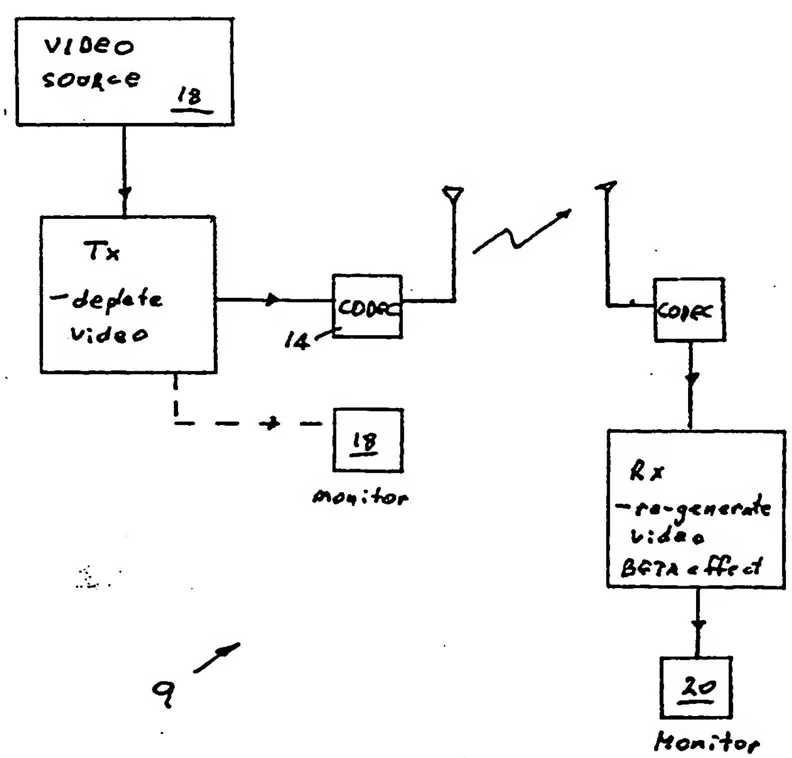
(54) Title: IMAGE PROCESSING SYSTEM

(57) Abstract

An image processing system (9) having a transmitter (10) capable of selecting a proportion of pixels (Umn) and deleting a proportion of pixels (Gmn, umn, gmn) of a video field for achieving data compression. A receiver (12) is provided for regenerating the deleted pixels (Gmn, umn, gmn) for regenerating the video field. The receiver (12) having a processor control (26a) for horizontally interlacing the regenerated pixels over a period of time substantially imperceptable to a viewer for relying upon the BETA APPARENT MOVEMENT effect for providing an apparent resolution which is greater than the actual resolution of the regenerated video field. Enhancement of the resolution of the video field is also provided by adding random noise pixels into the regenerated video field.



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TITLE

IMAGE PROCESSING SYSTEM

FIELD OF THE INVENTION

The present invention relates to an image processing system particularly, although not exclusively, envisaged for use in reducing the bandwidth requirements for transmission of video signals (i.e. for high definition television(HDTV), TV, video and video-phones), increasing the resolution of a video picture for a given bandwidth (HDTV) and in digitising signals for storage onto video cassette tapes.

The present invention is able to do this by taking into consideration the psychophysical attributes of the human visual perception system, namely BETA APPARENT MOVEMENT and SUPER EDGING (the Julesz stereopsis experiment).

BACKGROUND TO THE INVENTION

The design of the modern television has been influenced by previous discoveries in the cinema industry and are based on three basic design parameters:

1. Frame Format - in cinema it was discovered that a frame rate of 16 frames per second was needed to sustain smooth apparent motion. This was increased to 24 frames per second in order to reproduce sound. Then the rate was increased to half of the mains frequency (25 Hz in Europe and 30Hz in USA) so as to avoid mains interference.
2. Synchronisation - achieved by sequentially scanning video pictures starting at the top left of the frame and progressing to the bottom right on a line by line basis, and repeating the process for subsequent frames.
3. Flicker - which has important effects on selection of the frame frequency. If the frame frequency is too low (say 16 Hz or less) flicker results; at medium frequencies (say 25 Hz) stroboscopic effects are created (i.e. wheels appearing to

rotate counter to their actual movement; whereas at too high a frequency (50 Hz) the bandwidth required is too large and costs become prohibitive.

In relation to the latter, video compression techniques have been developed to reduce the bandwidth requirements. However, most of these solutions are based on algorithms which are mainly designed to detect and predict changes such as those described in the proposed CCITT standard H261.

Conventional display techniques including television and electronic displays work on the principle that for an image to be seen by a viewer, the complete image has to be represented by the illumination of the appropriate picture elements (pixels) in the form of the image. When these pixels are lit in their appropriate positions, the human eye can reconstruct the complete image, preserving the positional relationships of the pixels.

The biggest drawback of this method of display is that for images that require a higher level of resolution to be properly displayed (i.e. graphical images, including graphical company logos like Coca-Cola), a display consisting of a higher number of pixels is required. Similarly, for displays that scroll across the display screen to appear to be moving smoothly, large numbers of columns of these pixels are required, so that the resolution of the image, as it moves across the screen, can be preserved.

However, it was discovered that for moving objects, the human visual system is able to function perfectly on significantly less information than previously was assumed required. An example of this is an effect known as the BETA APPARENT MOVEMENT or picket fence effect, where an observer views a moving object through a picket fence that reveals no more than 10% of the object at any instant, yet the viewer is able to see the object perfectly. It is the movement of the object behind the picket fence which is

fundamental to the viewer being able to see the entire object.

Most drivers may notice that when moving (even at low speeds), the rails of bridges, low density vegetation, and the common picket fence become effectively transparent. Similarly, objects become quite visible through the spokes of rotating wheels, or the blades of rotating propellers.

In these cases, up to 90% of an object can be obscured by a moving obstacle, and still the full details of the object can be resolved. The converse also applies; a moving object can be shielded by a fixed a barrier which is up to 90% solid and the full details of he object can still be seen.

This is not due to the "persistence of vision", which in the past was ascribed to retinal retention. It is in fact due to the "BETA APPARENT MOVEMENT" effect. This effect is the correct reason for humans being able to interpret and connect different images into a sensation of motion. Conversely, the integration of partially presented images, scrolled over time, is also made possible by the same principle.

The BETA effect was used in Australian Patent No. 493435 where, instead of relying on large numbers of pixels in order to display graphical images of high resolution, the BETA effect was simulated and the human visual system was tricked into perceiving a resolution much higher than was actually being displayed.

In Australian Patent No. 493435 instead of using a display fully covered with pixels, a relatively small number of columns of pixels, spaced relatively far apart, were used (like the gaps in the fence that are the sole source of information). If the image is then moved across the display, either left to right or right to left, at a suitable rate, it was discovered that the human visual system would "fill in the gaps", giving the viewer the perception that the viewed image was being displayed at full resolution. The viewer thus would not notice that the image

at any given instant contained only a small fraction of the complete image. The process of deleting a significant portion of the image and regenerating it over time for recombination by the human visual system is herein referred to as "IMAGE DEPLETION" - the image was DEPLETED.

There are two main advantages to using image depletion. First, a display that only requires a column where every tenth column should be results in significant cost savings in the production and operation of such a display. Secondly, if this display is fed with information through an existing information network, significantly less information has to be transmitted for each "field" of the display to represent an image. This in turn has a two-fold advantage of either transmitting at a higher field rate than would be possible for the full non-depleted image, or transmitting on a network of narrower bandwidth than would otherwise be required for the non-depleted image.

The main problem with pictures, when stored and transmitted, is that they have a lot of data. Typically, an average television picture needs, when digitised, buffers running into millions of bytes. A PAL standard colour television picture needs three monochrome components, each of some 520,833 bytes. This image is assumed to have 625 x 625 = 390,625 pixels each with an aspect ratio of 4 x 3, add up to 520,833 bytes. The total, for a colour picture, equals three times this number, or approximately 1,562,500 bytes.

To send such a picture on a TV channel, the channel would need to be able to handle a rate of 1,562,500 x 8, or approximately 12.5 megabits, 25 times each second! This is equivalent to 12.5 x 25 i.e. 312.5 mega bit/sec.

The challenge is to reduce this data rate to the capabilities of ISDN network communication speeds of the order of 64 kb/sec.

The first step in handling such a huge task is to implement a system which can compress the picture, free it of any redundant information, and further reduce

transmission times by sending only the field and block differences rather than the whole field information. This is the intention of the proposed CCITT H261 JPEG/MPEG document covering the Discrete Cosine Transform (DCT), Motion Estimation Prediction (MEP) and ancillary algorithms.

Some of the reduction in transmission bandwidth requirement can be handled by these algorithms, but they have finite limits. We have discovered, however, that enhancement to picture quality, as well as reductions in transmission bandwidth requirement, can be achieved by **improving the machine-to-human interface by the use of Psychophysics.**

Prior art video systems (with the exception of Australian Patents 493435 and 573024) have been designed on the basis of a machine-to-machine interface and have not taken the special needs of the human perception system into consideration.

THE ROLE OF PSYCHOPHYSICS

In order to compress a video image for low bandwidth, we use the potential of the visual perception system of the observer to fill-in missing details. This requires a series of techniques which rely upon certain unique features in the manner in which the human brain functions. Hence, we can produce a considerable difference between actual and perceived resolution and so enhance the machine-to-human interface.

These techniques are chosen from:-

1. The BETA APPARENT MOVEMENT effect (the BETA effect);
2. Two dimensional interlacing;
3. Statistical fill-in; and,
4. Super Edging.

The latter two of which constitute a VISUAL ENHANCEMENT TECHNIQUE (VET).

The present invention relies on these techniques to enable considerable depletion of an image without causing significant loss of visual intelligibility of the image.

The BETA effect is used in a scanning and raster technique which works equally well whether the video image is stationary or moving and is referred to as a DEPLETION OPTIMISATION TECHNIQUE raster (DOT raster). The DOT raster adopts the BETA effect described in Australian patent 493435, except that, instead of requiring the video image to move with respect to a plurality of spaced apart stationary columns of video elements, a raster of columns are moved backwards and forwards with respect to a fixed or moving video image. Hence, the pixels are moved backwards and forwards to create apparent movement - even in still video images. This is equivalent to taking the picket fence analogy of Australian patent 493435 and moving the picket fence with respect to the video image instead of moving the video image with respect to the stationary picket fence. The effect can be simulated by closing one eye, spreading your fingers slightly apart and waving them in your field of view.

It is the movement of the column raster which enables the present invention to apply the BETA effect to a stationary video image. Also, a row raster can simultaneously be used to provide a horizontal depletion - to create a two dimensional interlace raster, as shown in Figure 1a.

In fact the raster movement of the pixels does not have to be limited to linear movement in rows and columns, but can be random in 2 dimensions, as shown in Figure 1b.

The DOT raster produces highly viewable video images even where the fields are reduced from 625 to 64 picture columns, each with only 128 out of 625 vertically arranged picture elements (pixels). This represents a horizontal depletion of 10:1 and a vertical depletion of 4:1, giving an overall depletion of 40:1. That is, each field is depleted by 40:1, but a time separated interlace of a plurality of the fields which build up a full video image having a resolution of 625 x 625 pixels.

Hence, the horizontal resolution which can be

achieved is not dependent upon the number of pixels in a single field, but is dependent on the number of unique positions that the DOT raster can acquire over time.

The columns can be broken up and rearranged into a two dimensional interlaced array (a checker board pattern as shown in Figures 2a, 2b and 2c). This has the effect of allowing the entire image to build up over a number of fields and to reduce the tendency for the viewer to lock onto the moving checker board.

Also, the DOT raster does not preclude the use of other data compression techniques such as Discrete Cosine Transform (DCT) and motion prediction algorithms. Hence, even greater savings in bandwidth are possible.

Further, statistical fill-in methods can be used to reduce any artefacts introduced into the video image by the DOT raster. This is achieved with a VISUAL ENHANCEMENT TECHNIQUE (VET) which relies on the injection of band limited noise into the video signal, once decoded, and manifests itself as pixels appearing between the other pixels of the decoded checker board pattern. The luminance value of the noise approximates that of the intensity of neighbouring pixels. This has the very surprising effect that the addition of noise increases the sharpness of the video image. Also, the injected noise creates pseudo pixels and hence can double the apparent resolution. As the noise does not have a fixed position within the DOT raster but is overlapped by true pixels, by the action of the Beta effect, the viewer perceives the average of the noise and active image.

The increase in sharpness can be explained by a consideration of the SUPER EDGING effect (see Figures 3a and 3b), where any random structure improves the sharpness of an image, this is the property of the viewer to "see" non-existent details between certain points. The edges of the shapes shown in Figures 3a and 3b appear extremely sharp even though the edges are formed from a random arrangement of pixels. The sharpness of the edges in these examples

would be unobtainable by simple connecting lines. It is the psychophysics of the human perception system which interpolates the random pixels and creates the perception of an extremely sharp edge - hence SUPER EDGING.

The ability of the viewer's visual perception system is such that, lacking full information, the missing information is "created" in dramatic detail. It is this ability which enables a viewer to appreciate "impressionistic" paintings. Further examples of the viewer "creating" the missing information to achieve a more complete image is shown in Figures 4a and 4b. In each case the viewer can perceive a triangle, yet if the spots are taken individually (by covering the other two) the viewer "sees" only what is present.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide an image processing system relying upon the BETA APPARENT MOVEMENT effect to enhance the perceived resolution of a video image.

In accordance with one aspect of the invention there is provided an image processing system having:

interlocking means for interlacing the pixels of subsequent fields of pixels horizontally;

whereby, the interlacing causes the pixels to move backwards and forwards at a rate substantially imperceptible to a human viewer for creating a perceived resolution of a video image formed by a plurality of the fields so interleaved, wherein the perceived resolution is greater than the actual resolution.

In accordance with another aspect of the invention there is provided an image processing system for compressing a video image referred to as an oniginal video image, the image processing system comprising:

a digitiser means for digitising the original video image, the original video image being formed of a plurality of original video fields each having M rows of pixels and N columns of pixels; and,

a process control means for processing the digitised original fields, the process control means selecting one pixel out of every d pixels and for deleting the remainder of the d-1 pixels for generating depleted fields in a depleted video image, the depleted field having m rows of pixels and n columns of pixels where m is less than M and n is less than N;

whereby, a receiver means can receive the depleted video image and can generate d-1 pixels from each selected pixel and can display each selected pixel and its associated d-1 generated pixels in a manner to simulate movement of the pixels on the display to substantially reconstruct the original video image by relying on the BETA APPARENT MOVEMENT effect.

In accordance with another aspect of the invention there is provided a method for compressing a video image referred to as an oniginal video image, the method comprising the steps of:

digitising a field of the original video image into a plurality of data bytes referred to as pixels, each original video field having M rows of pixels and N columns of pixels;

selecting one pixel out of every d pixels;

deleting the remainder of the d-1 pixels; and,

generating a depleted field of pixels in a depleted video image, the depleted field having m rows of pixels and n columns of pixels where m is less than M and n is less than N;

whereby, a receiver means can receive the depleted video image, generate d-1 pixels from each selected pixel and display each selected pixel and its associated d-1 generated pixels on a display means in a manner to simulate movement of the pixels to substantially reconstruct the original video image by relying on the BETA APPARENT MOVEMENT effect.

In accordance with another aspect of the invention there is provided an image processing system for decompressing a video image referred to as a depleted video

image, the image processing system comprising:

a digitiser means for digitising the depleted video image, the depleted video image being formed of a plurality of depleted video fields each having m rows of pixels and n columns of pixels; and,

a process control means for processing the digitised depleted fields, the process control means generating d-1 pixels from each selected pixel and displaying each selected pixel and its associated d-1 generated pixels over a period of time imperceptible to a viewer for simulating movement of the pixels on a display to regenerate an original video image having M rows of pixels and N columns of pixels;

wherein, the process controller relies upon the BETA APPARENT MOVEMENT effect in regenerating the original video image.

In accordance with another aspect of the invention there is provided a method for decompressing a video image referred to as a depleted video image, the method comprising the steps of:

digitising the depleted video image, the depleted video image being formed of a plurality of depleted video fields each having m rows of pixels and n columns of pixels;

selecting a pixel from the depleted video image;

generating d-1 pixels from each selected pixel;

displaying each selected pixel and its associated d-1 generated pixels over a period of time imperceptible to a viewer for simulating movement of the pixels on a display means for reconstructing an original video image with the selected pixels and the generated pixels, the reconstructed video image having M rows of pixels and N columns of pixels, where M is greater than m and N in greater than n;

wherein, the simulated movement relies upon the BETA APPARENT MOVEMENT effect in reconstructing the original video image.

Preferably, the luminance component of the injected noise is congruent with the luminance of adjacent pixels. Also, the injected noise is preferably band

limited.

Preferably, luminance determining means is provided to determine the luminance of the adjacent pixels and to set the luminance component of the pseudo pixel to a value proximate the actual value but different enough so as to induce an observer's perception system to select visually the most probable value.

BRIEF INTRODUCTION OF THE DRAWINGS

One embodiment, being an example only, of the present invention will now be described with reference to the accompanying drawings, in which:-

Figure 1a shows a two dimensional interlace of pixels, being in an ODD field "O" and an EVEN field "E";

Figure 1b shows a two dimensional random raster movement of pixels for a modulo-3 raster scheme;

Figures 2a to 2c show the break-up of a plurality of columns of video (Figure 2a) into a single depleted field (Figure 2b) and into two interlaced depleted fields (Figure 2c);

Figures 3a and 3b are diagrams showing the effect known as SUPER EDGING in relation to a square and a triangle;

Figures 4a and 4b are diagrams showing the effect known as FILLING-IN in relation to a triangle;

Figure 5 is a block diagram of an image processing system in accordance with the present invention;

Figure 6 is a block diagram of a receiver of the image processing system shown in Figure 5;

Figure 7 is a block diagram showing a transmitter of the image processing system shown in Figure 5;

Figure 8 is a graphical representation of a two interlaced regenerated fields U and G of the receiver shown in Figure 6; and,

Figure 9 shows a modulo-4 raster scheme.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The following relates to an embodiment of the image processing system 9 capable of providing a video depletion of about 40:1. The image processing system 9

comprises a transmitter 10 and a receiver 12, shown in Figures 6 and 7 respectively. A CODEC 14 is connected to an output of the transmitter 10 and another CODEC 16 is connected to an input of the receiver 12. A video source 18 is connected to an input of the transmitter 10 and a video monitor 20 is connected to an output of the receiver 12. Optionally, a monitor 21 is connected to the transmitter 10.

RECEIVER

The receiver 12 has a video signal conditioner 32a and a sync separator 32b connected to a video input 33 which is connected to the CODEC 16. The sync separator 32b is connected to a clock circuit 32c and a timing controller 32d which controls a clock timer 32e. The clock circuit 32c typically operates at a frequency of 12 megahertz and is hereinafter referred to as the "pixel clock" 32c. The video conditioner 32a is connected to an analogue digital converter 34a and thereby to a field store 34b. The output of the field store 34b is typically an 8-bit databus which is shown as a thick line in Figure 6. The field store 34b is connected to a delay circuit 34c and thereby to an 8-bit latch 34d. The delay of the delay circuit 34c is typically about 1 microsecond so as to enable correct syncing. The 8-bit latch 34d typically has a refresh rate of about 5 million times per second.

The sync and colour subcarrier components are extracted from the video signal at the video input 33 by a colour extractor 32 connected to the video input 33. The colour extractor 32 is connected to a colour processor 34 which typically includes a control circuit substantially the same as the remainder of the receiver 12. The colour extractor 34 operates on standard B-Y and R-Y signals sent in the video signal from the transmitter 10. Typically, the B-Y and R-Y signals are at a reduced resolution, such as half the resolution of the video signal processed by the pixel processor 26 (the compressed Y signal).

The analogue to digital converter 34a and the field store 34b digitise the video luminance signal from the

video conditioner 32a. The analogue to digital converter 34a generates digital values corresponding to the luminance of each pixel (hereinafter referred to as the "pixels") "on the fly" as the luminance signal is processed by the video conditioner 32a. The pixels are then stored in the appropriate memory address of the field store 34b. Typically, the luminance for each pixel is determined to be, for example, one of 256 luminance levels per pixel depending on the instantaneous voltage of the video signal (i.e. one in 2^8).

For ease of understanding the conception of the receiver consider that the field store 34b collects one full field of the luminance signal and stores it for further processing. That is, consider that the receiver 12 operates one field behind the incoming video signals at the video input 33.

The clock circuit 32c controls the timing of the analogue to digital converter 34a so as to digitise the signal received from the video conditioner 34a at the appropriate time to correspond to each pixel location of the video source 18. The sync separator 32b re-aligns the clock circuit 32c at the beginning of each line of the video signal by use of the horizontal sync signal contained therein.

The outputs of the field store 34b and the 8-bit latch 34d are connected to a pixel processor 36. The pixel processor 36 has a process controller 36a connected to latches and buffers 36c, 36d and 36e. The latch and buffer 36c is connected to an ALU unit 38c and thereby to a latch and buffer 38d. The clock timer 32e is connected to the 8-bit latch 34d, the latches and buffers 36c, 36d, 36e and 38d. The clock timer 32e combines the clock and sync signals from the sync separator 32b and the clock circuit 32c for controlling the timing of the pixel processor 36.

The process controller 36a reads the pixels from the field store 34b and allows them to proceed to the latch and buffer 36d. Also, the process controller 36a can allow

passage of the pixels to the latch and buffers 36c and 36e. The pixels which pass to the latch and buffer 36d correspond to those un-depleted pixels which were transmitted to the receiver 12.

A pseudo noise generator 38a is connected to the ALU unit 38c via a latch 38b. The pseudo noise generator 38a allows injection of noise pixels into the video image displayed on the monitor 20. The pseudo noise generator 38a typically generates pixels with luminance values which have a random value between the values of the adjacent pixels.

The outputs of the latches and buffers 36d, 36e and 38d are connected to a digital to analogue converter 40 which is connected to a video output 42 and hence to the monitor 20.

The pixel from the latches and buffers 36d, 36e and 38d are recombined with the colour information at the digital to analogue converter 40 via the colour processor 34 and with the sync information from the sync separator 32b hence forming a video signal corresponding to a regenerated video field for display on the monitor 20.

The process controller 36a reads pixels from the field store 34b one at a time in sequential order, corresponding to rows of the video signal from the video source 18 i.e. U11, U13,...U1,n (where n is the number of columns) as shown in Figure 8. However, once the pixels U11, U13...U1,n have been read the process controller 36a generates pixels G12, G14,...G1n-1 and sends them to the latch and buffer 36d before their each of associated pixels U11, U13,...U1n are sent to the latch and buffer 36d via the 8-bit latch 34d. That is, the generated pixel G12 is sent to the latch and buffer 36d before the depleted pixel U13 and so on. Hence, the process controller 36a generates the pixels between the un-depleted pixels from the video signal as it reads the un-depleted pixels and sends each generated pixel for display before it sends the last pixel read from the field store 34b to the latch and buffer 36d. The pixels are referred to as "un-depleted pixels" because they are the

pixels which remain after the depletion process of the transmitter 10, described hereinafter.

The control processor 36a generates the generated pixels G by considering the luminance values (between and 0 and 255) of the last two pixels read from the field store 34b and makes the generated pixel luminance value statistically dependent thereon. For example, the value of the generated pixel could be a polynomial interpolation of the values of the two un-depleted pixels.

Alternatively, the value could be a random value with the values of the two depleted pixels as its upper and lower limits. In this case the process controller passes control to the latch and buffer 36c and the pixel is generated by the pseudo noise generator 38a and sent to the DAC 40 via the latch and buffer 38d.

The process controller 36a then reads the pixels U31, U33,...U3,n of row three of the video image. These are the next pixels in the field store 34b. The control processor 36a also generates the pixels G32, G34,...G3n+1. Then the control processor 36a generates the pixels G21, G22,...G2n for the line of pixels between the first and third lines of pixels read from the field store 34b.

The effect of the above is that each depleted field commences with only 312 out of 625 pixels across and 312 out of 625 pixels down in each column but results in a full 625 line video signal. Hence, each depleted field had only one quarter of the pixels of the original field and the receiver 12 regenerates the other three quarters of the pixels, as shown graphically in Figure 8.

The above description relates to a modulo-2 depletion of the pixels of the original video signals. It amounts to a horizontal and vertical interlace of two fields, namely Un,m/Gn,m and un,m/gn,m.

The horizontal interlace has the effect of moving the image back and forth behind "a picket fence" and hence induces the BETA effect to give the illusion of higher than actual resolution to the viewer. The vertical interlace

gives higher vertical resolution.

In Figure 9 there is shown a graphical representation of a modulo-4 raster scheme. In modulo-4 four fields are effectively interlaced horizontally and step through positions marked "1" through "7". In this scheme the receiver 12 generates pixels G and g for three out of every four columns. Vertical interlacing could be included in this raster scheme. Further, as shown in Figure 1b the raster could be random (a random 2 dimensional modulo-3) in which over subsequent fields each pixel described the path shown by lines enumerated 1 to 9.

TRANSMITTER

The transmitter 10 has a transmission signal conditioner 22a and a since separator 22b connected to a video input 23 which is driven by the video source 18 (such as a video camera or HDTV program or VCR or the like). The sync separator 22b is connected to a clock circuit 22c and a timing controller 22d which controls a clock timer 22e. The clock circuitry 22c typically operates at a frequency of 12 megahertz and is hereinafter referred to as the pixel clock 22c. The video conditioner 22a is connected to an analogue digital converter 24a and thereby to a field store 24b. The output of the field store 24b is typically an 8-bit databus which is shown as a thick line in Figure 7. The field store 24b is connected to a delay circuit 24c and thereby to an 8-bit latch 24d. The delay of the delay circuit 24c is typically about 1 microsecond so as to enable correct syncing. The 8-bit latch 24d typically has a refresh rate of about 5 million times per second.

The signal conditioner 22a extracts the luminance component from the video signal. A colour extractor 22 extracts the colour component from the video signal received from the video source 18. The colour extractor 22 is connected to a colour processor 27 which typically includes a control circuit substantially the same as the remainder of the transmitter 10. The colour extractor 27 operates on standard B-Y and R-Y signals sent in the video signal from

the transmitter 10. Typically, the B-Y and R-Y signals are at a reduced resolution, such as half the resolution of the video signal processed by the pixel processor 26 (the compressed Y signal).

The analogue to digital converter 24a and the field store 24b digitise each field received from the video source 18 and store it for digital processing. The analogue to digital converter 24a generates digital values of the luminance of each pixel (hereinafter referred to as "pixels") "on the fly" as the luminance signal is processed by the video conditioner 22a. Typically, the luminance is determined to be, for example, one of 256 luminance levels per pixel (i.e. one in 2^8).

The clock circuit 22c controls the timing of the analogue to digital converter 24a so as to digitise the signal received from the video conditioner 24a at the appropriate time to correspond to each pixel location of the video source 18. The sync separator 22b re-aligns the clock circuit 22c at the beginning of each line of the video signal by use of the horizontal sync signal contained therein.

The output of the field store 24b and the 8-bit latch 24d is connected to a pixel processor 26. The pixel processor 26 has a process controller 26a connected to latches and buffers 26c and 26d. The latch and buffer 26c is connected to an ALU unit 28a and thereby to a latch and buffer 28b. The clock timer 22e is connected to the 8-bit latch 24d and the latches and buffers 26c, 26d and 28b. The clock timer 22e combines the clock and sync signals from the sync separator 22b and the clock circuit 22c for controlling the timing of the pixel processor 26.

The process controller 26a reads luminance values from the field store 24b one at a time in sequential order, corresponding to rows of the video signal from the video source 18.

For ease of understanding the conception of the transmitter consider that the field store 24b collects one

full field of the luminance signal and stores it for further processing. That is, consider that the transmitter 10 operates one field behind the incoming video signals at the video input 23.

Referring to Figure 8 the process controller 26a selects, for example, the pixels corresponding to the ODD rows and the ODD columns, i.e. Un,m for all values of n and m. These pixels are referred to as the "un-depleted pixels" and are allowed to proceed to the latch and buffer 26d for transmission to the receiver 12. Also, the process controller 26a allows passage of other ones of the pixels the latch and buffer 26c. These pixels are referred to as "depleted pixels". The pixels which pass to the latch and buffer 26c are used to be displayed on a monitor 15 by the ALU unit 28a, the latch and buffer 28b and a digital to analogue converter 31. The digital to analogue converter 31 is also connected to an output of the latch and buffer 26d and therefore, the monitor 15 can show a video signal similar to that which will be shown on the monitor 20 at the receiver 12.

A pseudo noise generator 28c is connected to the ALU unit 28a via a latch 28d. The pseudo noise generator 28c allows injection of noise pixels into the video image displayed on the monitor 15.

The process controller 26a has the effect of, for example, selecting ODD pixels from ODD video fields and EVEN pixels from EVEN video fields. The combined effect is a field having two fields which are interlaced both horizontally and vertically as shown in Figure 8. That is, every second column and every second row from the original video signal has been deleted. Hence, the resultant video signal for transmission is referred to as "depleted".

The output of the latch and buffer 26d is connected to a digital to analogue converter 30 which is connected to the CODEC 14 for transmission via, for example, an antenna. The sync separator 22b is connected to the DAC 30 to control its timing.

The effect of the above is that each field is depleted from 625 down to 312 pixels across and from 625 down to 32i pixels down in each column. Hence, each depleted field has one quarter of the information of the original field. This corresponds to a modulo-2 depletion of the pixels of the original video signals.

The luminance of the depleted pixels is recombined with the sync and colour information at the digital to analogue converter 30 via the colour processor 27 and the sync separator 22b respectively.

As with the receiver 12 other forms of depletion of the video signal could be used, such as, for example, modulo 3, 4, 5 etc. or even a relatively random form of depletion as shown in Figure 1b in which over subsequent fields each pixel describes the path shown by lines 1 to 9. This is a two dimensional version of modulo-3.

In modulo-4, as shown in Figure 9, each field image is digitised and saved in the field store 24b in the following manner:

- during field 1, starting from the first pixel, only 1 pixel in 8 is saved on each line. The displayed picture looks similar to Figure 2a where part of a 64 column pattern is depicted;
- during field 2, starting from pixel 3, only the three-modulo-8 elements are saved;
- during fields 3 and 4 the same process is used for pixel 5 and 7 respectively.

The combined effect is a frame of 4 fields that looks similar to Figure 2b, in which every second line has been deleted - both horizontally and vertically.

The image processing system of the present invention allows for considerable compression of a video signal by relying on the psychophysical attributes of the human perception system to undertake appropriate interpolation of the video image to provide a perceived resolution which is substantially the same as that of the uncompressed signal - even though the actual resolution has

been severely depleted. The DOT system relies on the BETA APPARENT MOTION effect to achieve the high compression by deletion of all information from the video signal which is not necessary for the human perception system. The BETA effect is achieved in still video images by moving the pixels, such as, backwards and forwards. Also, the viewability of the interlaced fields is enhanced due to the very high statistical correlation - between the pixels of subsequent fields (by stepping the pixels backwards and forwards). The VET then adds random noise to the signal, once received, in order to make the resultant video image sharper - by relying on the phenomenon of SUPER EDGING. Also, the system of the present invention preferably operates in a digital format and so avoids analogue artefacts (i.e. overshoot and smear) which are very difficult to remove. Statistical manipulation of the video signal can allow for even greater compression. For example, the video signal, as compressed by the DOT raster, could be processed by a DCT to give a further compression of 40:1, thus giving a total compression of 1600:1. Hence, a video signal can be compressed and transmitted via a telephone line having a bandwidth of 64kHz - thus being applicable to video telephone without requiring special or multiple telephone lines.

Also, the DOT can be used to enhance the resolution of a standard video signal to achieve a high definition video result. And, such high definition can be achieved simply by processes at the receiver. Still further, the DOT could be used to digitise video signals for video recorders and video cameras.

Modification and variations such as would be apparent to a skilled addressee are considered within the scope of the present invention. For example, other systems of movement of the pixels could be used to take advantage of the BETA effect e.g. circular or random movement of pixels.

CLAIMS

1. An image processing system having:

interlocking means for interlacing the pixels of subsequent fields of pixels horizontally;

whereby, the interlacing causes the pixels to move backwards and forwards at a rate substantially imperceptible to a human viewer for creating a perceived resolution of a video image formed by a plurality of the fields so interleaved, wherein the perceived resolution is greater than the actual resolution.

2. An image processing system according to claim 1, in which the interlacing means interlaces pixels horizontally and vertically.

3. An image processing system according to claim 1, in which the interlacing means interlaces the pixels in a random manner.

4. An image processing system according to any one of the preceding claims, also comprising a noise generation means for generating pixels of random luminance for interspersing between the pixels for relying upon the super edging effect for enhancing the perceived resolution of the video image.

5. An image processing system for compressing a video image referred to as an original video image, the image processing system comprising:

a digitiser means for digitising the original video image, the original video image being formed of a plurality of original video fields each having M rows of pixels and N columns of pixels; and,

a process control means for processing the digitised original fields, the process control means selecting one pixel out of every d pixels and for deleting the remainder of the d-1 pixels for generating depleted fields in a

depleted video image, the depleted field having m rows of pixels and n columns of pixels where m is less than M and n is less than N;

whereby, a receiver means can receive the depleted video image and can generate d-1 pixels from each selected pixel and can display each selected pixel and its associated d-1 generated pixels in a manner to simulate movement of the pixels on the display to substantially reconstruct the original video image by relying on the BETA APPARENT MOVEMENT effect.

6. An image processing system according to claim 5, in which the process controller interlaces the pixels in a random manner.

7. A image processing system according to claim 5, also comprising a noise generation means for generating pixels of random luminance for interspersing between the pixels for relying upon the super edging effect for enhancing the perceived resolution of the video image.

8. A method for compressing a video image referred to as an original video image, the method comprising the steps of:

digitising a field of the original video image into a plurality of data bytes referred to as pixels, each original video field having M rows of pixels and N columns of pixels;

selecting one pixel out of every d pixels;

deleting the remainder of the d-1 pixels; and,

generating a depleted field of pixels in a depleted video image, the depleted field having m rows of pixels and n columns of pixels where m is less than M and n is less than N;

whereby, a receiver means can receive the depleted video image, generate d-1 pixels from each selected pixel and display each selected pixel and its associated d-1 generated pixels on a display means in a manner to simulate

movement of the pixels to substantially reconstruct the original video image by relying on the BETA APPARENT MOVEMENT effect.

9. An image processing system for decompressing a video image referred to as a depleted video image, the image processing system comprising:

a digitiser means for digitising the depleted video image, the depleted video image being formed of a plurality of depleted video fields each having m rows of pixels and n columns of pixels; and,

a process control means for processing the digitised depleted fields, the process control means generating d-1 pixels from each selected pixel and displaying each selected pixel and its associated d-1 generated pixels over a period of time imperceptible to a viewer for simulating movement of the pixels on a display to regenerate an original video image having M rows of pixels and N columns of pixels;

wherein, the process controller relies upon the BETA APPARENT MOVEMENT effect in regenerating the original video image.

10. An image processing system according to claim 9, also comprising a noise generation means for generating pixels of random luminance for interspersing between the pixels for relying upon the super edging effect for enhancing the perceived resolution of the video image.

11. A method for decompressing a video image referred to as a depleted video image, the method comprising the steps of:

digitising the depleted video image, the depleted video image being formed of a plurality of depleted video fields each having m rows of pixels and n columns of pixels;

selecting a pixel from the depleted video image;

generating d-1 pixels from each selected pixel;

displaying each selected pixel and its associated d-1

generated pixels over a period of time imperceptible to a viewer for simulating movement of the pixels on a display means for reconstructing an original video image with the selected pixels and the generated pixels, the reconstructed video image having M rows of pixels and N columns of pixels, where M is greater than m and N in greater than n;

wherein, the simulated movement relies upon the BETA APPARENT MOVEMENT effect in reconstructing the original video image.

12. An image processing system according to claim 11, also comprising a noise generation means for generating pixels of random luminance for interspersing between the pixels for relying upon the super edging effect for enhancing the perceived resolution of the video image.

o = odd field pixel display
e = even field pixel display

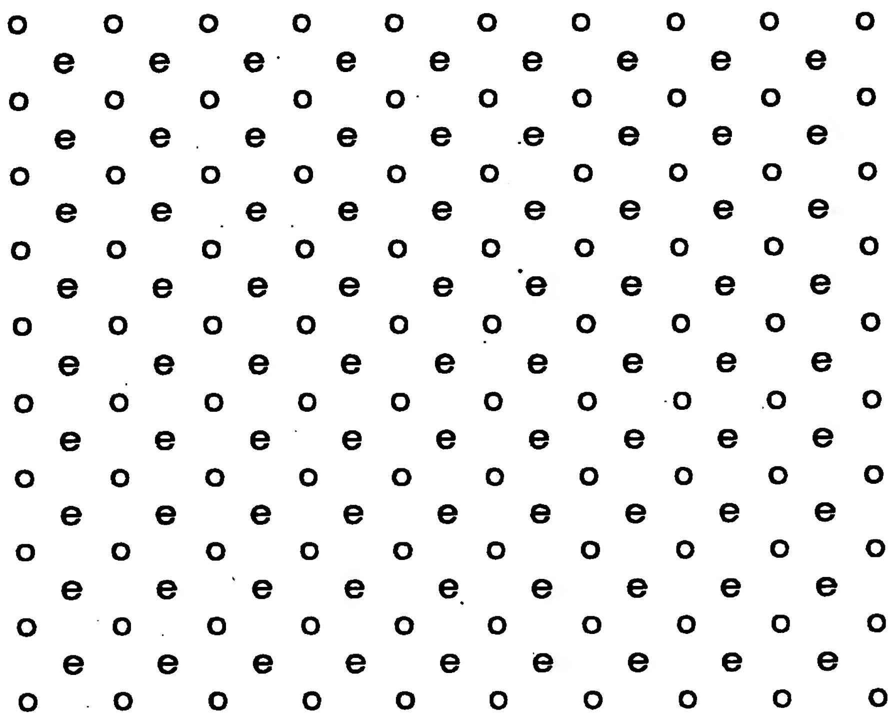


Fig 1a

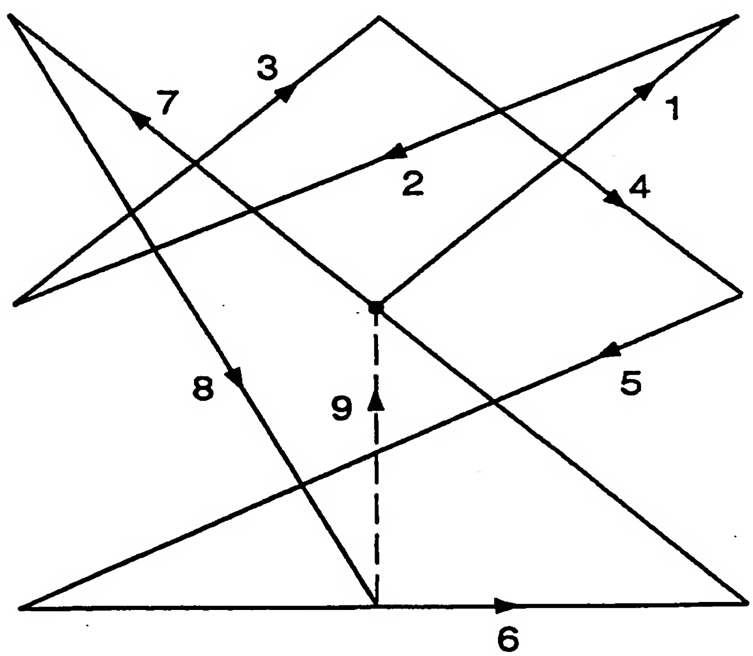


Fig 1b

FIG 2a

FIG 2b

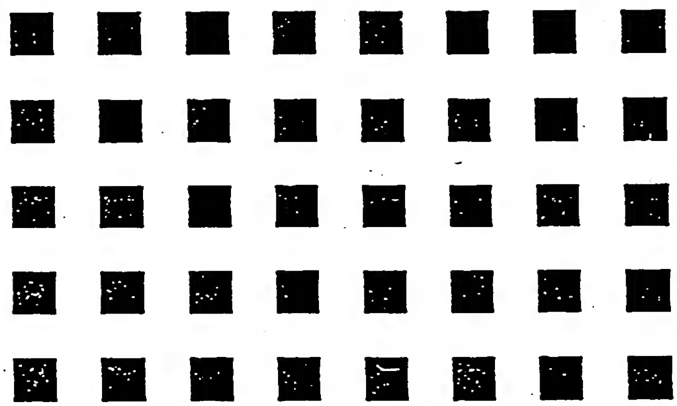
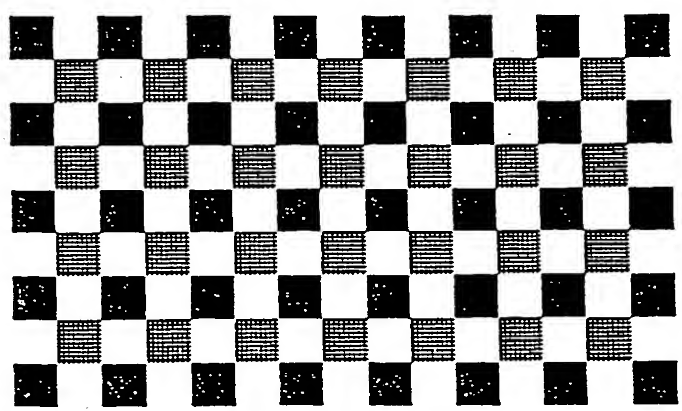


FIG 2c



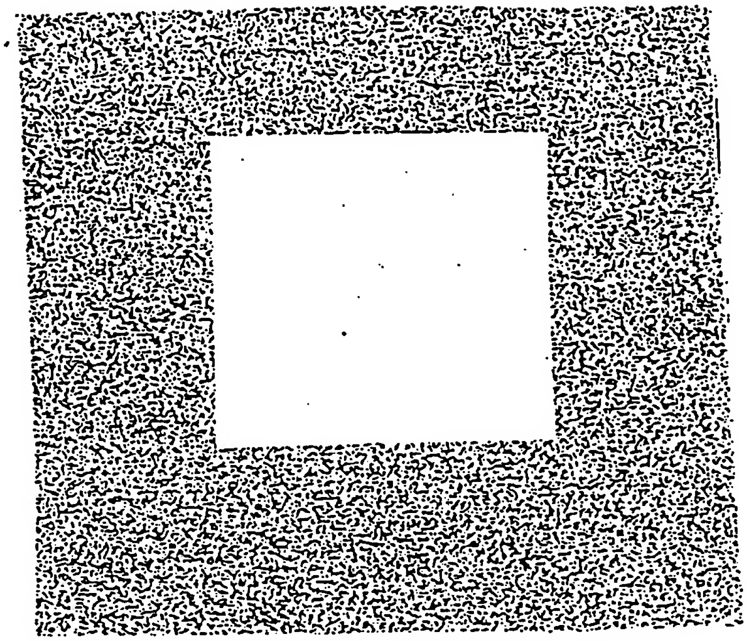


FIG 3a

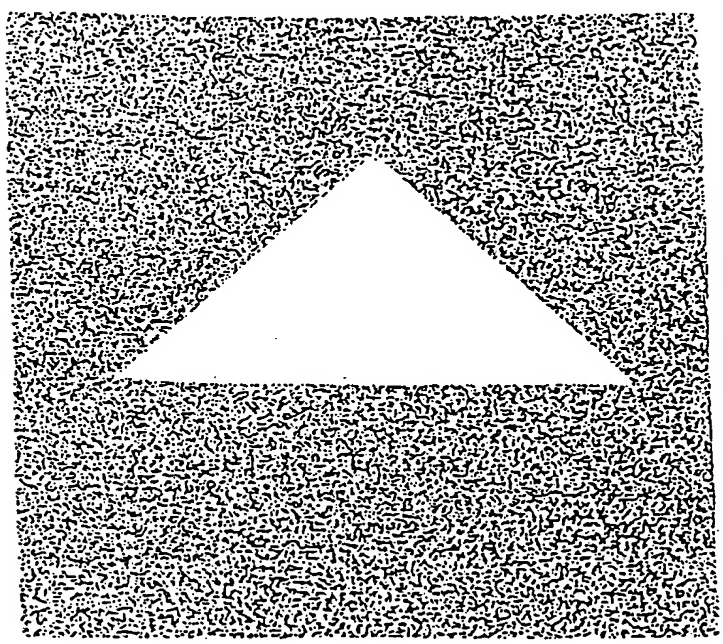


FIG 3b

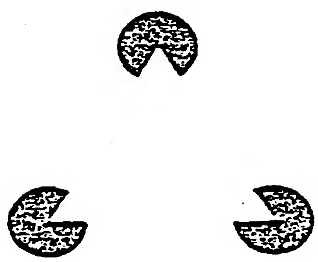


Figure 4a

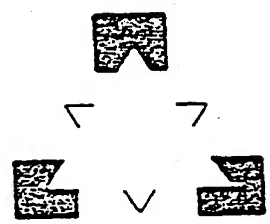


Figure 4b

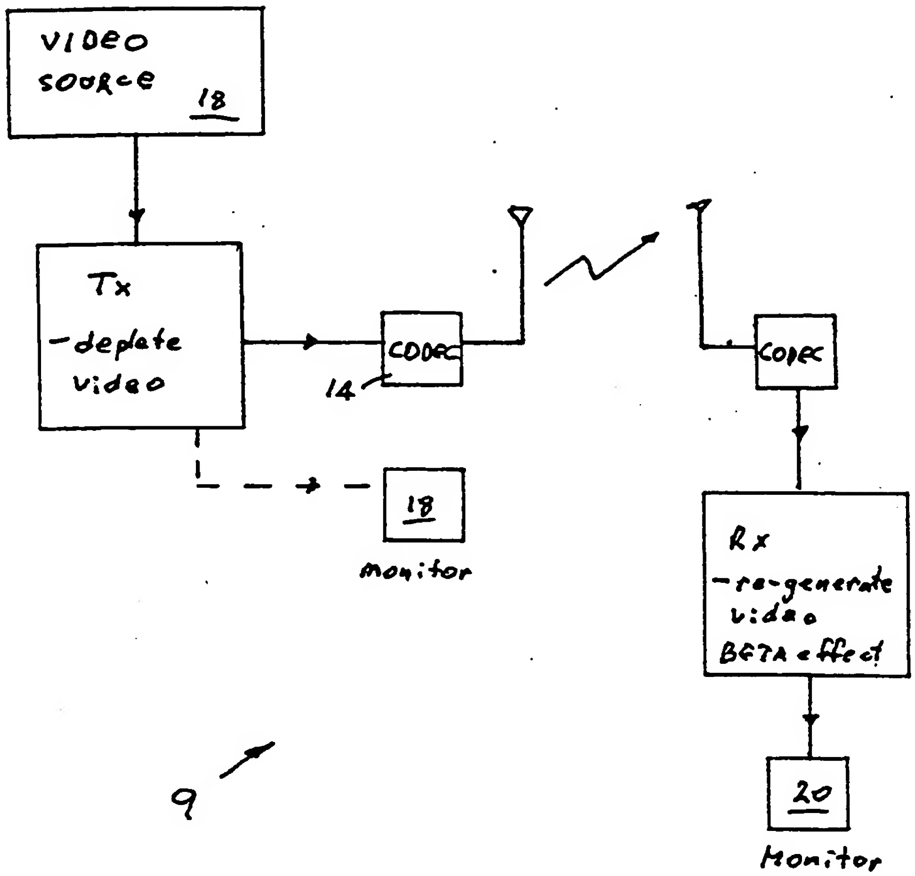

VIDEO
SOURCE
18
Tx
-deplete
video
CODEC
14
18
monitor
CODEC
Rx
-re-generate
video
BETA effect
20
Monitor
9

FIG. 5.

FIG 6

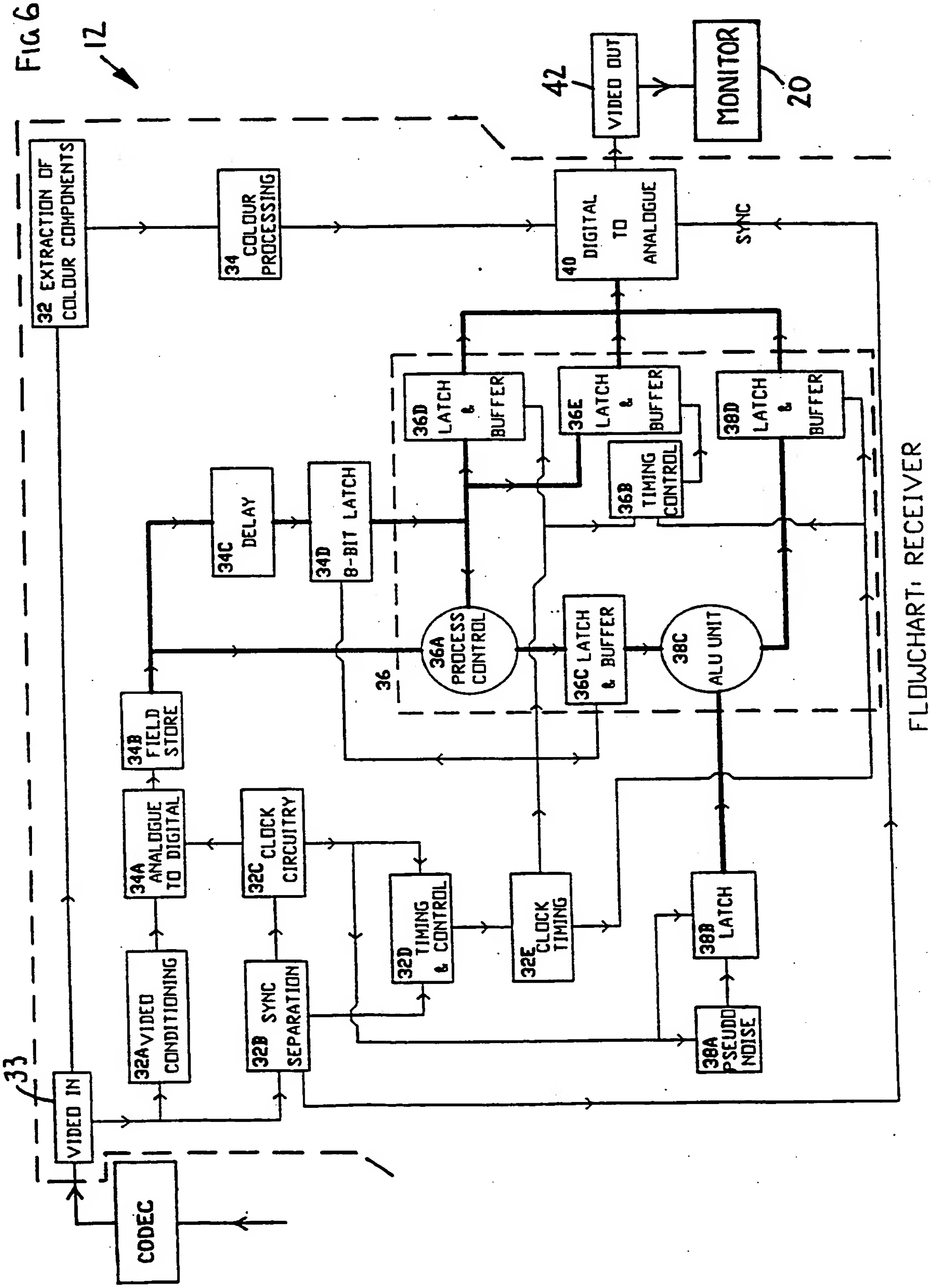
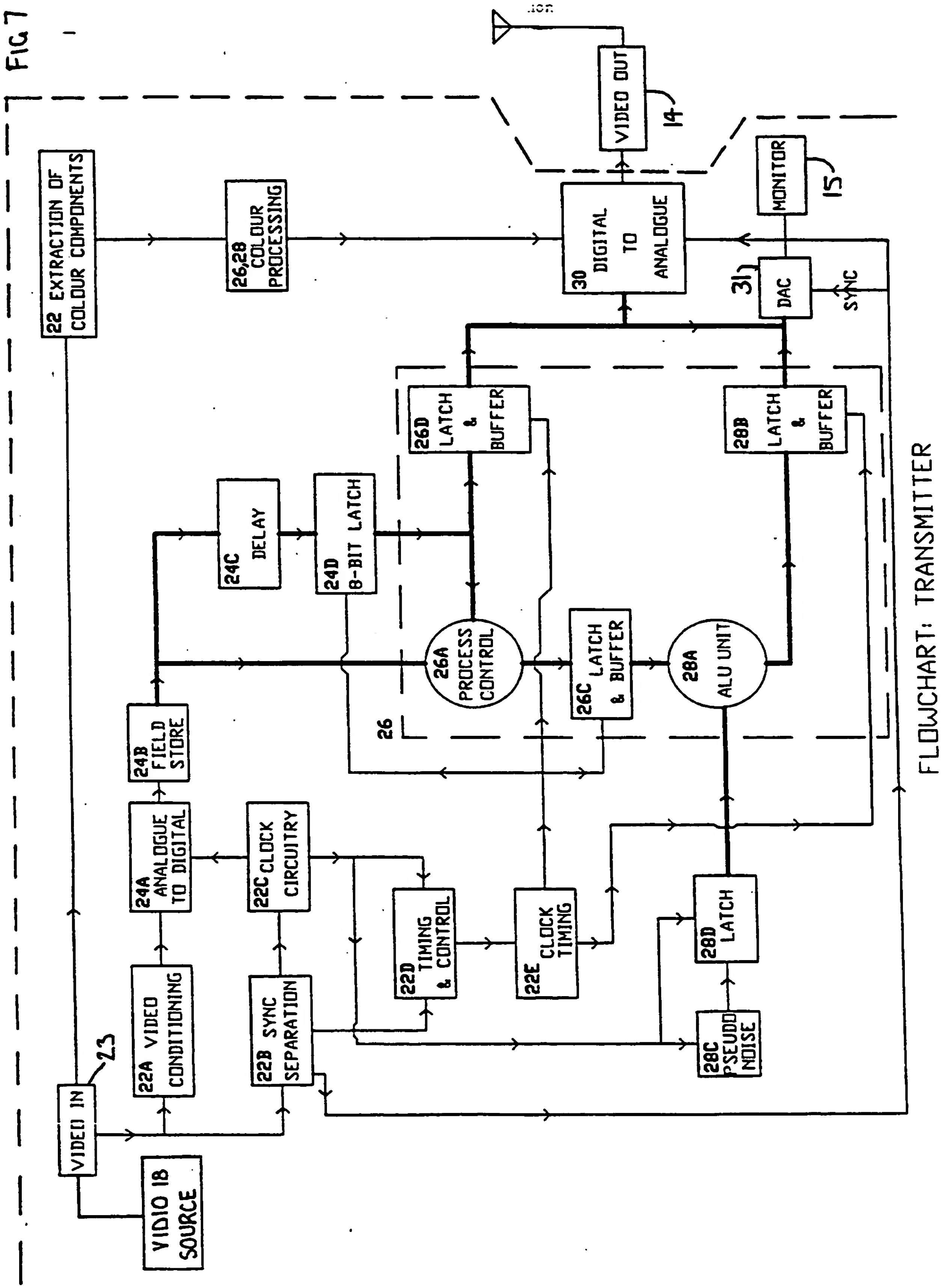

12
33
VIDEO IN
CODEC
32A VIDEO CONDITIONING
32B SYNC SEPARATION
32C CLOCK CIRCUITRY
32D TIMING & CONTROL
32E CLOCK TIMING
34A ANALOGUE TO DIGITAL
34B FIELD STORE
34C DELAY
34D 8-BIT LATCH
32 EXTRACTION OF COLOUR COMPONENTS
34 COLOUR PROCESSING
36
36A PROCESS CONTROL
36B TIMING CONTROL
36C LATCH & BUFFER
36D LATCH & BUFFER
36E LATCH & BUFFER
38A PSEUDO NOISE
38B LATCH
38C ALU UNIT
38D LATCH & BUFFER
40 DIGITAL TO ANALOGUE
SYNC
42
VIDEO OUT
MONITOR
20
FLOWCHART: RECEIVER

FIG 7


22 EXTRACTION OF COLOUR COMPONENTS
26,28 COLOUR PROCESSING
30 DIGITAL TO ANALOGUE
VIDEO OUT
14
MONITOR
15
31
DAC
SYNC
26D LATCH & BUFFER
28B LATCH & BUFFER
24C DELAY
24D 8-BIT LATCH
26A PROCESS CONTROL
26C LATCH & BUFFER
28A ALU UNIT
26
24B FIELD STORE
24A ANALOGUE TO DIGITAL
22C CLOCK CIRCUITRY
22D TIMING & CONTROL
22E CLOCK TIMING
28D LATCH
22A VIDEO CONDITIONING
22B SYNC SEPARATION
28C PSEUDO NOISE
VIDEO IN
23
VIDIO 18 SOURCE
FLOWCHART: TRANSMITTER

U11	u11	G12	g12	U13	u13	G14	g14	U15	u15	G16	g16	U17	u17	G18	g18	U19	u19
G21	g21	G22	g22	G23	g23	G24	g24	G25	g25	G26	g26	G27	g27	G28	g28	G29	g29
U31	u31	G32	g32	U33	u33	G34	g34	U35	u35	G36	g36	U37	u37	G38	g38	U39	u39
G41	g41	G42	g42	G43	g43	G44	g44	G45	g45	G46	g46	G47	g47	G48	g48	G49	g49
U51	u51	G52	g52	U53	u53	G54	g54	U55	u55	G56	g56	U57	u57	G58	g58	U59	u59
G41	g61	G42	g62	G43	g63	G44	g64	G45	g65	G46	g66	G47	g67	G48	g68	G49	g69
U71	u71	G72	g72	U73	u73	G74	g74	U75	u75	G76	g76	U77	u77	G78	g78	U79	u79
G81	g81	G82	g82	G83	g83	G84	g84	G85	g85	G86	g86	G87	g87	G88	g88	G89	g89
U91	u91	G92	g92	U93	u93	G94	g94	U95	u95	G96	g96	U97	u97	G98	g98	U99	u99

U - first field, un-depleted pixel

G - first field, generated pixel

u - second field, un-depleted pixel

g - second field, generated pixel

FIG. 8.

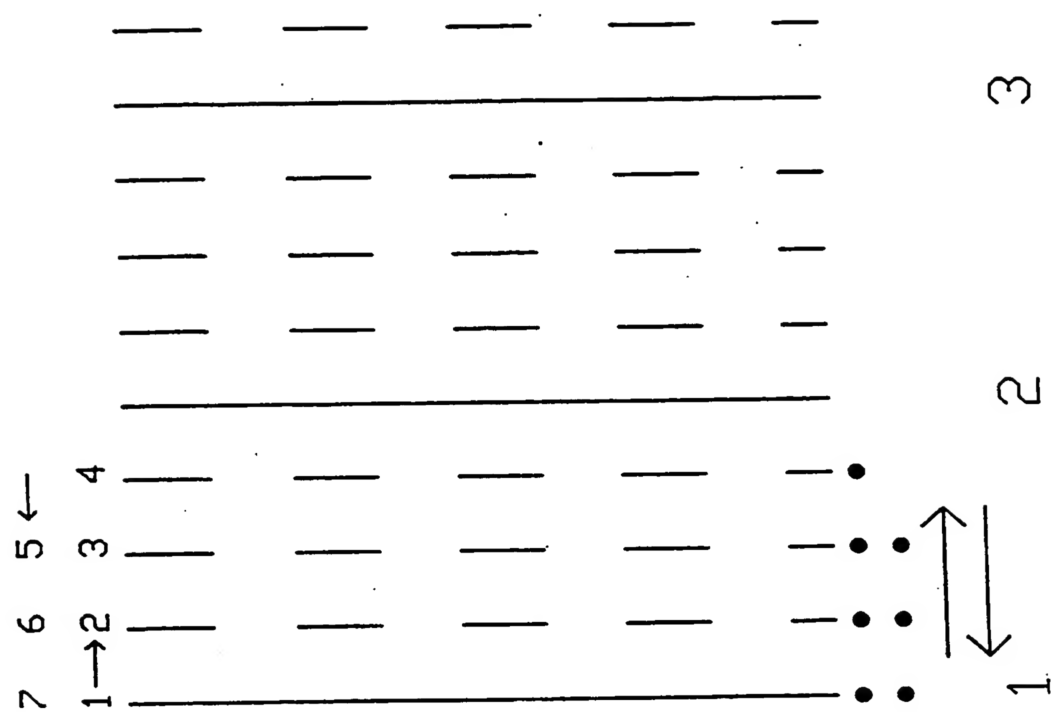


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 93/00368

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.^{5} H04N 7/12, 7/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC H04N 7/12, 7/13

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU : IPC as above

Electronic data base consulted during the international search (name of data base, and where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
X	US,A, 2479880 (TOULON) 8 August 1946 (08.08.46) entire document	1,2
X	US,A, 3136847 (BROWN) 9 June 1964 (09.06.64) entire document	1,2
X	US,A, 3566023 (SMIERCIAK) 23 February 1971 (23.02.71) column 2 lines 14-36, Figs 1,8	1,2
X	US,A, 3586775 (SMIERCIAK) 22 June 1971 (22.06.71) column 2 lines 31-69, Figs 1,3,4	1-3

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 November 1993 (03.11.93)	5 NOV 1993 (5.11.93)

Name and mailing address of the ISA/AU	Authorized officer
AUSTRALIAN INDUSTRIAL PROPERTY ORGANISATION PO BOX 200 WODEN ACT 2606 AUSTRALIA	P.P. Gerondal P.P. GERONDAL
Facsimile No. 06 2853929	Telephone No. (06) 2832184

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate of the relevant passages	Relevant to Claim No.
X	US,A, 4068265 (RUSSELL) 10 January 1978 (10.01.78) column 1 line 33 - column 2 line 4, column 2 line 59 - column 3 line 63, Figs 1,2	1
X	GB,A, 1232108 (INTERNATIONAL STANDARD ELECTRIC CORPORATION) 19 May 1971 (19.05.71) entire document	1,2
X	GB,A, 1236749 (INTERNATIONAL STANDARD ELECTRIC CORPORATION) 23 June 1971 (23.06.71) entire document	1,2
X	GB,A, 1250226 (INTERNATIONAL STANDARD ELECTRIC CORPORATION) 20 October 1971 (20.10.71) entire document	1-3
A	EP,A, 0146713 (NIPPON HOSO KYOKAI) 3 July 1985 (03.07.85) page 14 line 1 - page 15 line 23, Fig 2	
A	EP,A, 0174056 (NAGOYA UNIVERSITY) 12 March 1986 (12.03.86) page 4 line 9 - page 6 line 1, page 7 line 3 - page 16 line 11, Figs 2-4	

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	3566023	FR	1582586	GB	1236749	JP	48013247
US	3586775	AT	302429	BE	729100	DE	1908871
		FR	2002760	GB	1250226	NL	6903223
GB	1232108	FR	1582585				
GB	1236749	FR	1582586	JP	48013247	US	3566023
GB	1250226	AT	302429	BE	729100	DE	1908871
		FR	2002760	NL	6903223	US	3586775
EP	146713	JP	60054008	CA	1213359	DE	3479953
		US	4745459	JP	60086994	JP	60153682
		JP	60163577				
EP	174056	DE	3583980	JP	61062286	US	4675733

END OF ANNEX